PATENT APPLICATION
Do. No. 9898-206

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Shin KIM, et al.

Serial No. 10/068,628 Examiner: Dinh, Tuan T

Confirmation No. 6784

Filed: February 6, 2002 Group Art Unit: 2827

For: SEMICONDUCTOR DEVICE BONDING PAD RESISTANT TO STRESS AND METHOD OF FABRICATING THE SAME

BOX NON FEE AMENDMENT
Assistant Commissioner for Patents
Washington, D.C. 20231

RESPONSE TO OFFICE ACTION

Responsive to the Office Action, dated August 14, 2002, please amend the application as follows.

IN THE SPECIFICATION

Please replace the paragraph at page 5, line 30 to page 6, line 2, with the following:

Reference numerals 106′, 110, and 114 denote a second dielectric layer, an inter-metal dielectric layer (IMD), and a passivation layer, respectively. These layers are dielectric layers used to sequentially form the second metal layer 112, the first metal layer 108, and the polysilicon film plate 104.

IN THE CLAIMS

1. (Once amended) A bonding pad of a semiconductor device, said bonding pad comprising:

a substructure formed on a semiconductor substrate;

a first dielectric layer formed on the substructure;

a polysilicon film plate formed on the first dielectric layer;

a second dielectric layer formed overlying the polysilicon film plate, the second dielectric layer having a first opening that expose a region of the polysilicon film plate,

a first metal layer formed on the polysilicon film plate through the first opening;

an inter-metal dielectric (IMD) layer formed overlying the first metal layer, the inter-metal dielectric layer having a second opening that exposes a region of the first metal layer;

a second metal layer formed on the first metal layer in the second opening; and

a passivation layer formed overlying the second metal layer, the passivation layer having a third opening that exposes a region of the second metal layer as a bonding pad.

2. A bonding pad according to claim 1, wherein the first metal layer is formed having a somewhat horseshoe-shaped cross-section.

3. A bonding pad according to claim 2, wherein a region of the second metal layer is disposed within a recessed area of the first metal layer.

4. A bonding pad according to claim 1, wherein the second metal layer has a somewhat horseshoe-shaped cross-section.

5. A bonding pad according to claim 1, wherein the substructure comprises circuitry configured to provide a dynamic random access memory.

6. A bonding pad according to claim 1, wherein the first dielectric layer is a boron phosphor silicate glass (BPSG) layer.

7. A bonding pad according to claim 1, wherein the first dielectric layer has a thickness of between about 3000-4000 Å.

8. A bonding pad according to claim 1, wherein the polysilicon film plate has a thickness of about 1000-2000 Å.

9. A bonding pad according to claim 1, wherein the first and second metal layers are formed of aluminum.

10. A bonding pad according to claim 1, wherein the first metal layer has a thickness of approximately 7000-7500 Å.

11. A bonding pad according to claim 1, wherein the second metal layer has a thickness of about 8500-9000 Å.

12. A bonding pad according to claim 1, wherein the wire bonding is beam lead bonding.

13. A semiconductor package comprising a semiconductor chip having the bonding pad of claim 1.

14. A semiconductor package module having a semiconductor chip mounted thereon, wherein the semiconductor chip comprises a bonding pad according to claim 1.

20. (Once amended) A bonding pad of a semiconductor device, said bonding pad comprising:

a substructure formed on a semiconductor substrate;

a first dielectric layer formed on the substructure;

a polysilicon film plate formed on the first dielectric layer and configured to improve the resistance of the bonding pad to stress created during wire bonding;

a first metal layer formed on the polysilicon film plate, wherein the first metal layer is formed having a recessed area;

a second metal layer formed on the first metal layer, wherein a portion of the second metal layer is arranged within the recessed area of the first metal layer to improve the resistance of the bonding pad to stress; and

a passivation layer formed overlying the second metal layer having an opening that exposes the second metal layer as a bonding pad.

21. (New) A bonding pad according to claim 20, wherein the substructure comprises a gate dielectric layer and a gate electrode sequentially formed on the semiconductor substrate, the substructure includes source/drain regions formed adjacent to the gate electrode.

REMARKS

Claims 1-20 are pending in the application. Claims 15-19 are withdrawn from consideration.

Claims 1-5, 9, 12-14 and 20 rejected under 35 U.S.C. 102(b) as being anticipated by Zambrano (U.S. Patent 5,773,899).

Claims 6-8, and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zambrano (U.S. Patent 5, 773,899) in view of Fukumoto (U.S. Patent 6,307,264).

Claims 1 and 20 are amended.

New claim 21 is added. The limitation of new claim 21 is supported in the specification, for example, at page 6, lines 11-13.

No new matter is added.

Claims 1-14 and 21 remain in the case for reconsideration.

Applicants request reconsideration and allowance of the claims 1-14 and 21 in light of the following remarks.

Claim Rejections – 35 USC § 102

Claims 1-5, 9, 12-14 and 20 rejected under 35 U.S.C. 102(b) as being anticipated by Zambrano.

The rejection is respectfully traversed.

Claim 1 is amended to recite:

"a substructure formed on a semiconductor substrate;

a first dielectric layer formed on the substructure;

a polysilicon film plate formed on the first dielectric layer;

a second dielectric layer formed overlying the polysilicon film plate, the second dielectric layer having a first opening that expose a region of the polysilicon film plate;

a first metal layer formed on the polysilicon film plate through the first opening;

an inter-metal dielectric (IMD) layer formed overlying the first metal layer, the inter-metal dielectric layer having a second opening that exposes a region of the first metal layer;

a second metal layer formed on the first metal layer in the second opening; and

a passivation layer formed overlying the second metal layer, the passivation layer having a third opening that exposes a region of the second metal layer as a bonding pad."

Zambrano does not, however, teach or disclose the above features recited in claim 1. For example, Zambrano does not teach or disclose "a passivation layer formed overlying the

second metal layer, the passivation layer having a third opening that exposes a region of the second metal layer as a bonding pad."

On the contrary, in the Zambrano reference, a second metal layer 16 is formed over a layer of passivating material 13. See col. 3, lines 44-49 of the Zambrano reference. Rather, Zambrano teaches away from the present invention because "no additional passivating layers are necessary, since the surface of the semiconductor is already protected by the layer 13" according to the teachings of the Zambrano reference. See col. 3, lines 52-54 of the Zambrano reference. Thus, a person skilled in the art would not form a passivation layer over the second metal layer 16 upon reading the Zambrano reference, as recited in claim 1 of the present application.

For these reasons, Zambrano does not teach or disclose all of the limitations of claim 1 and, thus, does not anticipate claim 1. Thus, claim 1 is allowable.

Also, claims 2-5, 9, 12-14, which depend from allowable claim 1 and recite features that are not taught or disclosed in the cited reference, are also allowable. For example, with respect to claim 5, the Zambrano reference merely states that "It is evident...the process...is not limited in its application to power MOSFETs or PICs, but can be employed in the manufacturing of any otherpower semiconductor deice, such as Insulated Gate Bipolar Transistors ((IGBTs)." Such *power* semiconductor devices are different from and are not a dynamic random access memory, as recited in claim 5. Further, in the Zambrano reference, bonding wires 17 and 18 are not beam lead bondings, but just conventional bond wires. Nothing in Zambrano teaches or suggests that the wires 17 and 18 are lead bondings as recited in claim 12. Additionally, the Zambrano reference does not teach or disclose "A semiconductor package comprising a semiconductor chip having the bonding pad of claim 1," or "A semiconductor package module having a semiconductor chip mounted thereon, wherein the semiconductor chip comprises a bonding pad according to claim 1," as recited in claims 13 and 14, respectively.

Similar to claim 1, claim 20 is also amended to recite limitations, "a passivation layer formed overlying the second metal layer having an opening that exposes the second metal layer as a bonding pad." Thus, claim 20 is also allowable for the reasons discussed above.

Claim Rejections – 35 USC § 103

Claims 6-8, and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zambrano in view of Fukumoto .

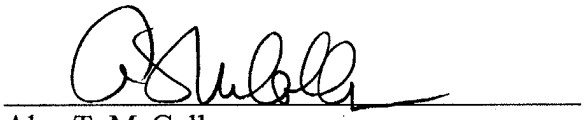
The rejection is respectfully traversed.

As discussed above, Zambrano does not teach or disclose all of the limitations of claim 1. Thus, the rejection does not present a *prima facie* case of obviousness. Accordingly, claims 6-8 and 10-11, which depend from allowable claim and recite features that are neither taught nor disclosed in the cited references, are also allowable.

For the foregoing reasons, reconsideration and allowance of claims 1-14 and 21 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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